Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) A gallium nitride based heterojunction field effect transistor device comprising:
a substrate;
a buffer region positioned upon said substrate, wherein said buffer region comprises an upper buffer region and a lower buffer region;
a heterojunction region positioned upon said buffer region; and
a superlattice positioned between said lower buffer region and said upper buffer region, wherein said superlattice comprises individual layers of GaN and $Al_xGa_{1-x}N$;
~~wherein said device is configured to function as a heterojunction field effect transistor.~~

2. (original) The device of claim 1, wherein x is from about 0.01 to about 0.40.

3. (original) The device of claim 2, wherein x is from about 0.02 to about 0.30.

4. (original) The device of claim 1, wherein said superlattice comprises from about 2 to about 500 individual layers.

5. (original) The device of claim 4, wherein said superlattice comprises from about 5 to about 100 individual layers.

6. (original) The device of claim 1, wherein said lower buffer region is about 0.1 to about 3 μm thick.

7. (original) The device of claim 6, wherein said lower buffer region is about 0.2 to about 0.5 μm thick.

8. (original) The device of claim 1, wherein said individual layers of said superlattice are from about 5 to about 200 Å thick.

9. (original) The device of claim 1, wherein said heterojunction region comprises a first layer and second layer, wherein said second layer is positioned directly above said upper buffer region, and said first layer is positioned directly above said second layer.

10. (original) The device of claim 9, wherein said first layer and said second layer both comprise $Al_yGa_{1-y}N$, where y has a value of from about 0.1 to 1.

11. (original) The device of claim 10, wherein said first layer is doped and said second layer is undoped.

12. (original) The device of claim 11, wherein said first layer has a thickness of from about 100 to 300 Å, and said second layer has a thickness of from about 2 to 30 Å.

13. (original) The device of claim 1, wherein said heterojunction region comprises $Al_bGa_{1-b}N$, where b has a value of from about 0.1 to 1.

14. (original) The device of claim 13, wherein said $Al_bGa_{1-b}N$ is pulse doped.

15. (original) The device of claim 14, wherein said pulse doped $Al_bGa_{1-b}N$ has a trilayer structure with a layer of dopant with a thickness of about 2 to 10 Å between two layers of undoped $Al_bGa_{1-b}N$.

16. (original) The device of claim 1, wherein said substrate comprises silicon.

17. (currently amended) A gallium nitride based heterojunction field effect transistor device comprising:

a substrate comprising sapphire;

a buffer region positioned upon said substrate, wherein said buffer region comprises an upper buffer region and a lower buffer region;

a heterojunction region positioned upon said buffer region; and

a superlattice positioned between said lower buffer region and said upper buffer region, wherein said superlattice comprises individual layers of GaN and $Al_xGa_{1-x}N$;

~~wherein said device is configured to function as a heterojunction field effect transistor.~~

18. (original) The device of claim 17, wherein x is about 0.28.

19. (original) The device of claim 17, wherein said superlattice comprises from about 4 to about 50 individual layers.

20. (original) The device of claim 19, wherein said superlattice comprises about 10 individual layers.

21. (original) The device of claim 17, wherein said lower buffer region comprises at least one layer of AlN, and at least one layer of GaN.

22. (currently amended) The device of claim 21, wherein said at least one layer of GaN is about 0.4 μm thick, and said at least one layer of AlN is about 300 Å thick.

23. (original) The device of claim 17, wherein said GaN layers of said superlattice are about 80 Å thick, and said $Al_xGa_{1-x}N$ layers are about 100 Å thick.

24. (currently amended) A gallium nitride based heterojunction field effect transistor device comprising:

a substrate comprising silicon carbide;

a buffer region positioned upon said substrate, wherein said buffer region comprises an upper buffer region and a lower buffer region;
a heterojunction region positioned upon said buffer region; and
a superlattice positioned between said lower buffer region and said upper buffer region, wherein said superlattice comprises individual layers of GaN and $Al_xGa_{1-x}N$.~~;~~
~~wherein said device is configured to function as a heterojunction field effect transistor.~~

25. (original) The device of claim 24, wherein x is about 0.02.

26. (original) The device of claim 24, wherein said superlattice comprises from about 4 to about 50 individual layers.

27. (original) The device of claim 26, wherein said superlattice comprises about 10 individual layers.

28. (original) The device of claim 24, wherein said lower buffer region comprises at least one layer of AlN, and at least one layer of GaN.

29. (currently amended) The device of claim 28, wherein said at least one layer of GaN is about 0.4 μm thick, and said at least one layer of AlN is about 1000 Å thick.

30. (original) The device of claim 24, wherein said GaN layers of said superlattice are about 80 Å thick, and said $Al_xGa_{1-x}N$ layers are about 100 Å thick.